EE 435

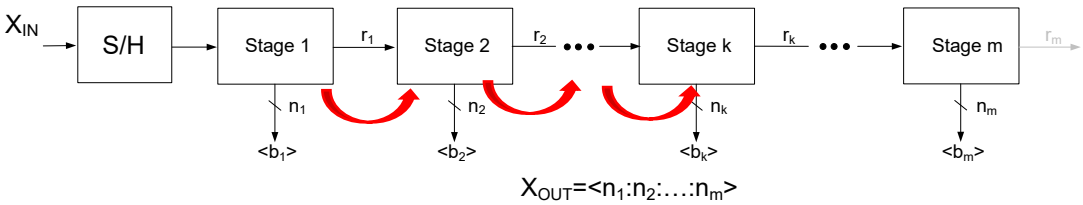
Lecture 40

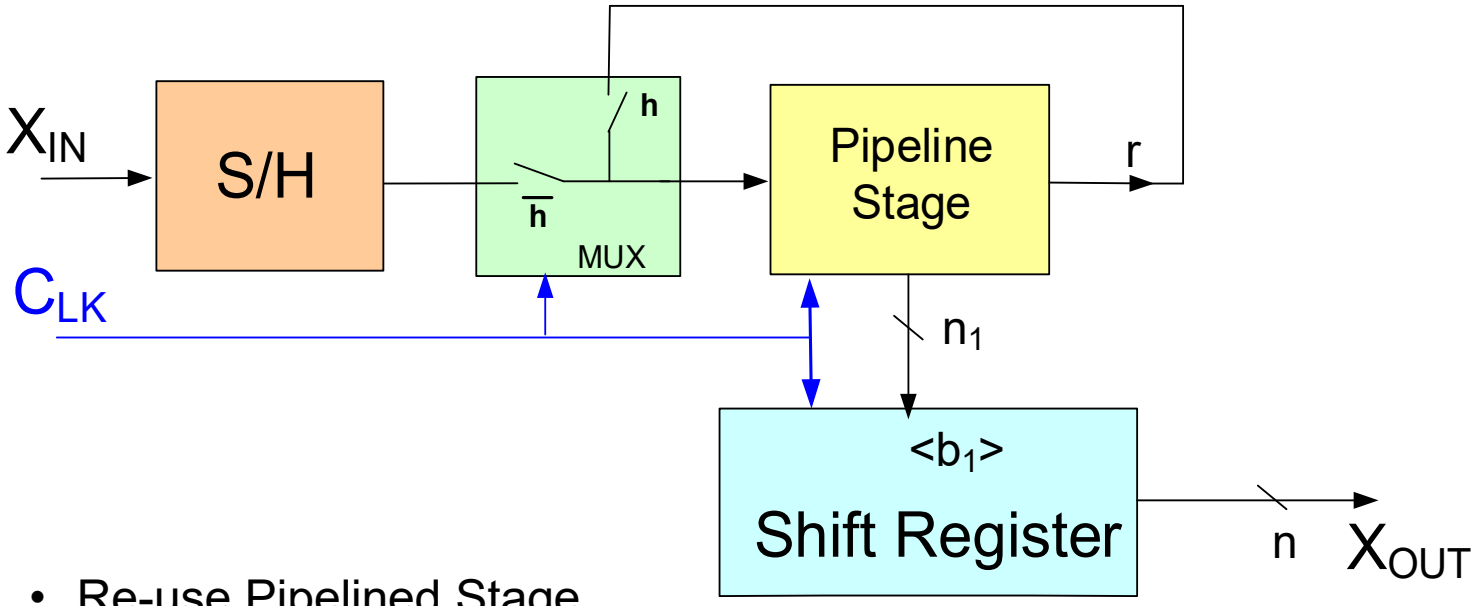
Data Converters

- Noise

Review from Last Lecture

Cyclic (Algorithmic) ADC

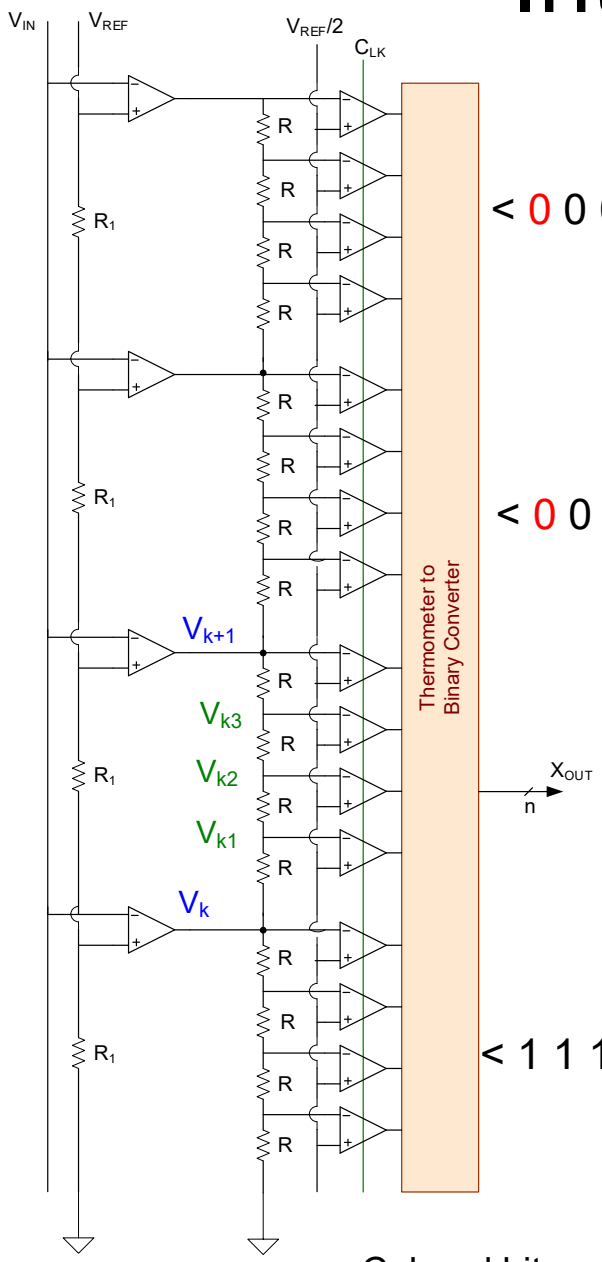




- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases

Review from Last Lecture

Interpolating ADC

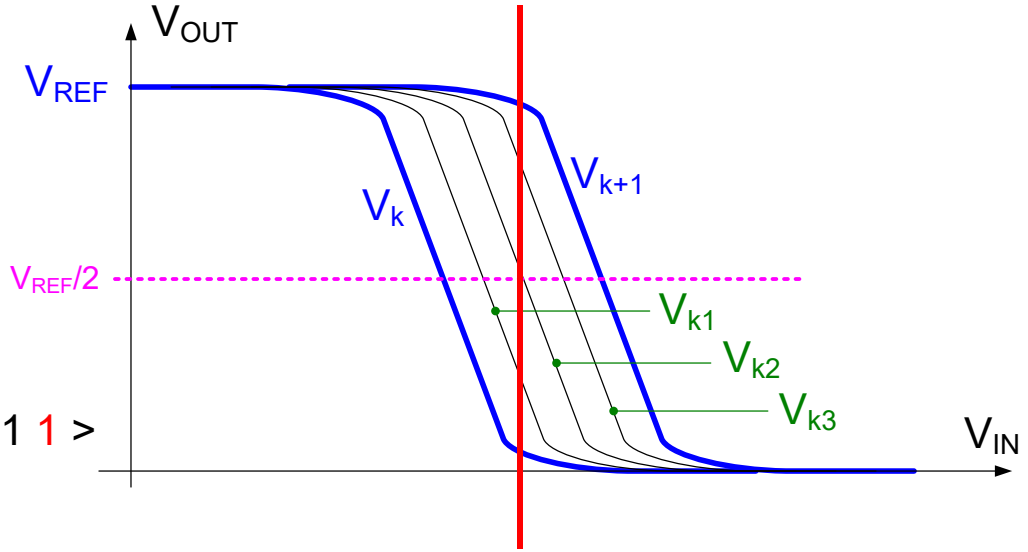


< 0 0 0 0 0 >

< 0 0 0 0 0 >

< 1 1 1 1 1 >

- Amplifiers are finite-gain saturating
- Amplifiers need not be accurate or linear
- Shown for 4-bit
- Same common-mode input on comparators
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators

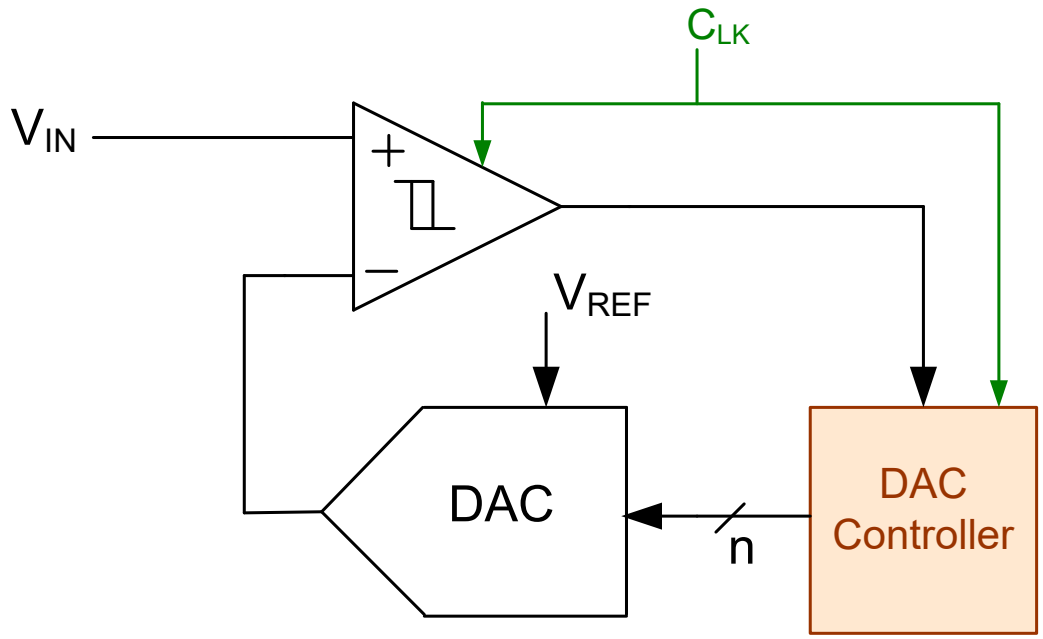


< 1 1 0 0 0 >

Colored bits are shared

Review from Last Lecture

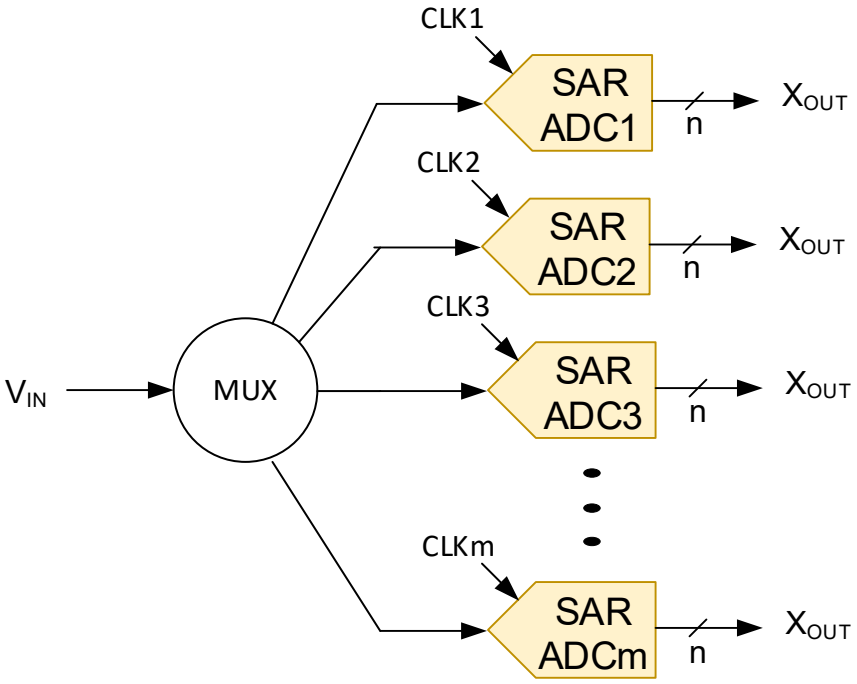
SAR ADC



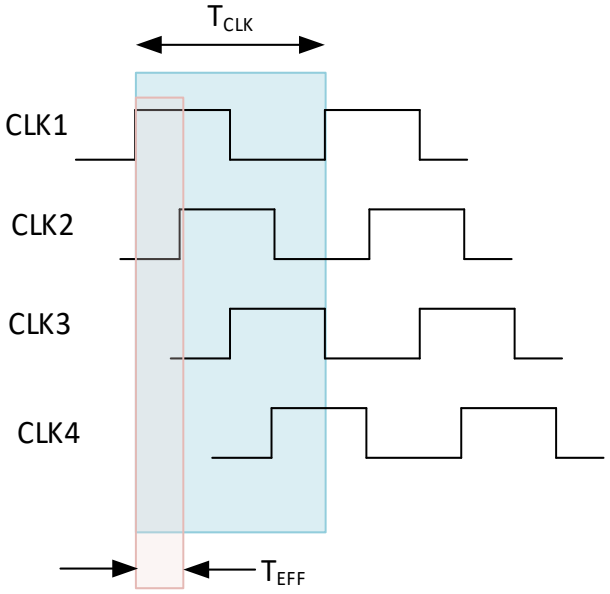
- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small
- Any DAC can be used
- Single comparator !

Review from Last Lecture

Time Interleaved SAR ADC

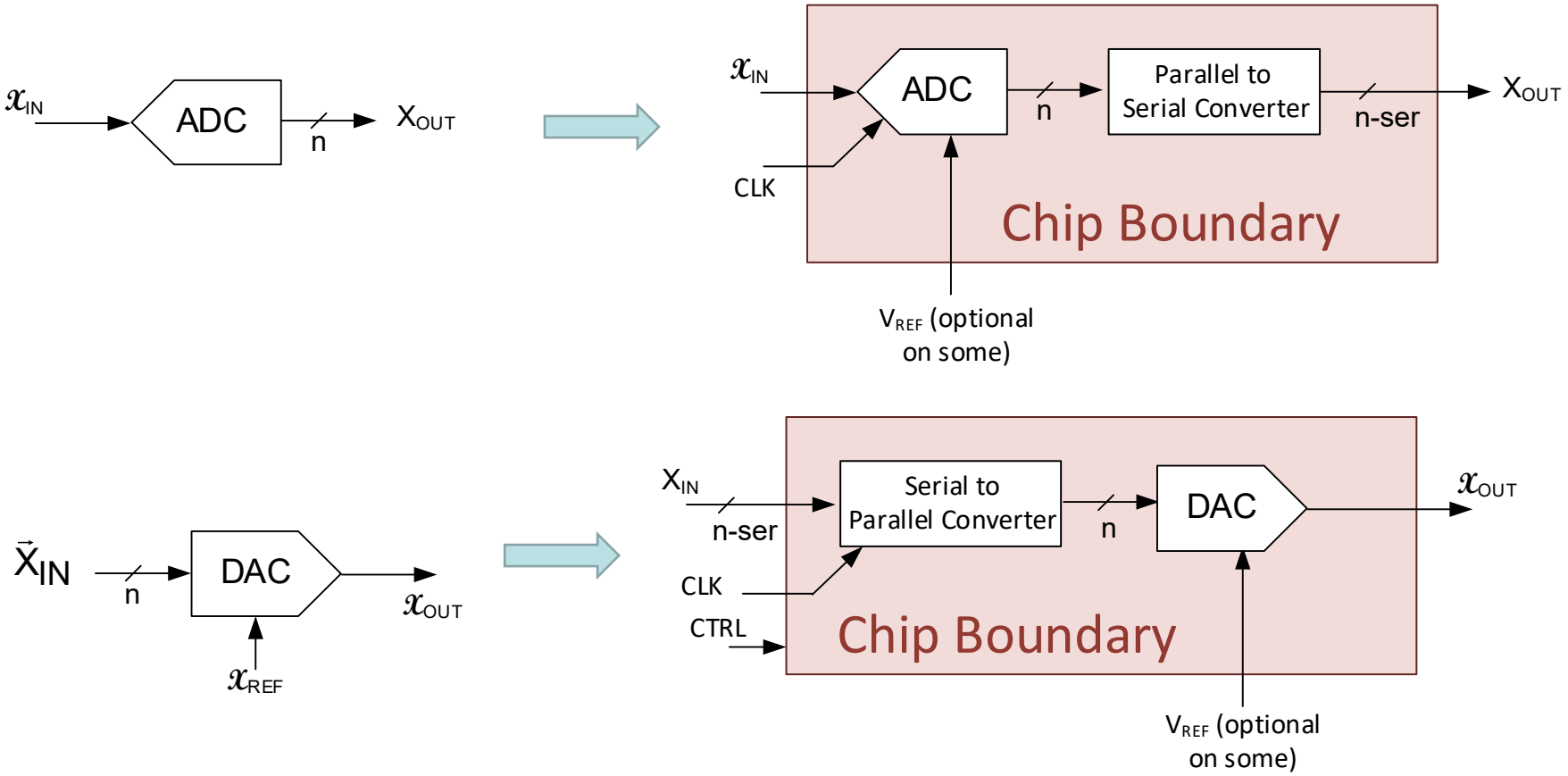


Time interleaving increases effective conversion rate by factor of m



Actual Catalog Data Converter Parts

- Often (not always) digital interface with data converter is serial
- Significantly Reduces pin count
- Interfaces usually follow standard protocols
- Challenge in data converter design almost always in the data converter itself
- Multiple channels often available and these usually use single converter and MUX



Common Application

Want digital representation of analog input at a “distant” location

Distance could be a few cm or thousands of miles

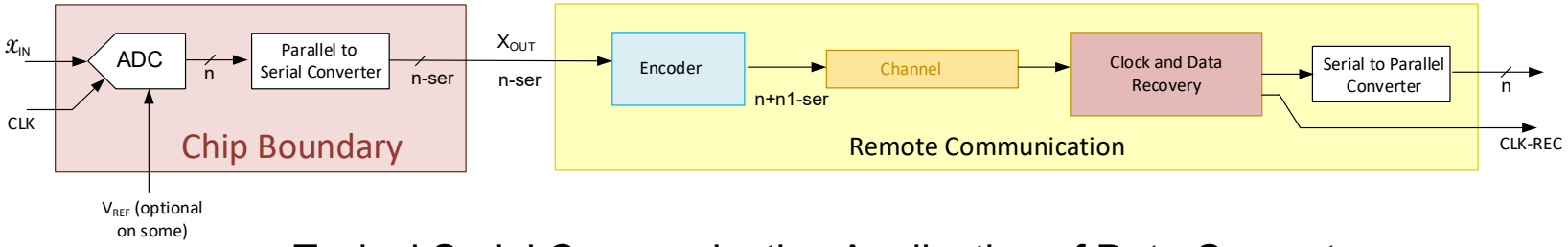
Transmitting clock would dramatically increase communication overhead and provide no additional information

Keeping phase of clock aligned with data would be extremely difficult even for short distances

Data is usually encoded and at receiver end both clock and data are recovered (CDR)

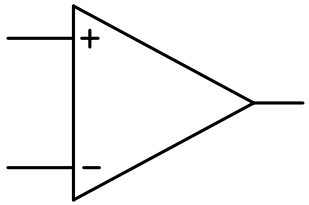
Digital signals themselves degrade when passing through channel

Bit overhead is significant



Typical Serial Communication Application of Data Converter

Noise in ADCs and DACs

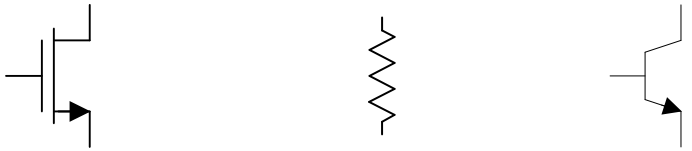


Noise in electronic devices and components introduce noise in electronic systems

Noise is of major concern in ADCs, DADs, and Op Amps

Beyond the scope of this course to go into lots of details about effects of device noise in these components but will provide a brief introduction

Devices that contribute noise :

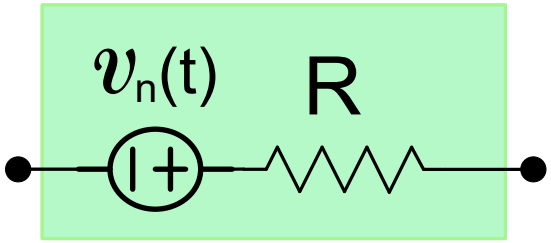


Capacitors and Inductors are noiseless:

Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in resistors:



Noise can be characterized by either $v_n(t)$ (time domain)
or the spectral density S (frequency domain)

Noise spectral density of $v_n(t)$ at all frequencies for a resistor

$$S = 4kTR$$

k: Boltzmann's Constant
T: Temperature in Kelvin

$k=1.38064852 \times 10^{-23}\ m^2\ kg\ s^{-2}\ K^{-1}$

At 300K, $kT=4.14 \times 10^{-21}$

This is termed white noise because S is independent of f !

Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in linear circuits:

$$v_n(t) \iff S(f)$$

Typically interested in RMS value of the noise voltage v_{RMS}

Time domain:

$$v_{RMS} = \sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{t=0}^{T} v_n^2(t)\,dt}$$

Difficult to obtain directly !

Frequency domain:

$$\tilde{v}_{RMS} = \sqrt{\int_{f=0}^{\infty} S(f)\,df}$$

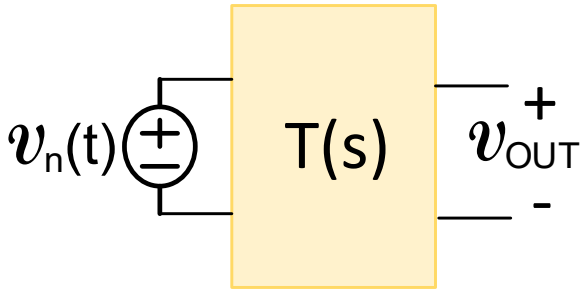
It can be shown that:

$$\tilde{v}_{RMS} = v_{RMS}$$

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in linear circuits:



Due to any noise voltage source:

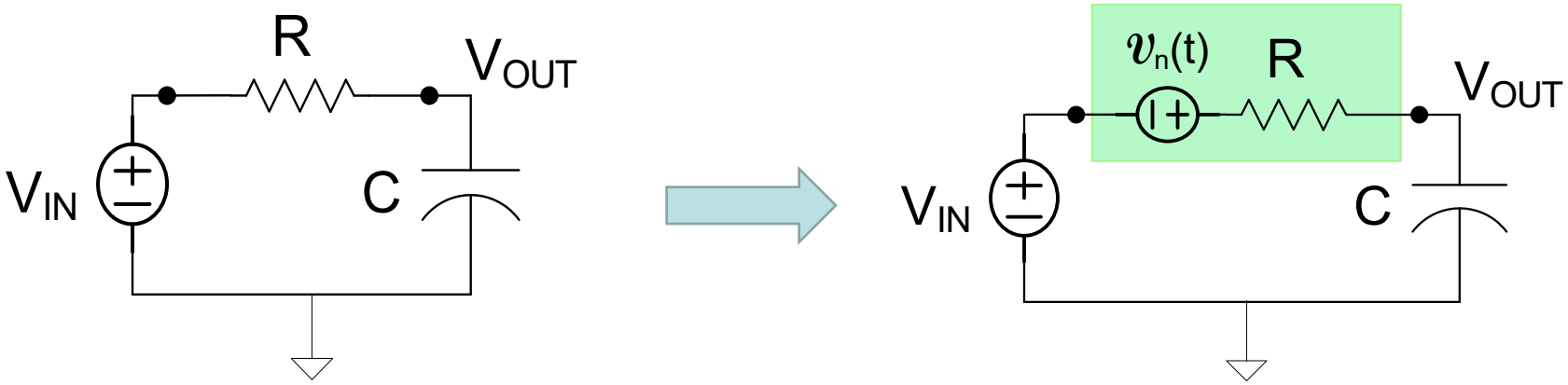
$$S_{V_{OUT}} = S_{V_n} \left| T_n(j\omega) \right|^2$$

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df}$$

Thus:

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \sqrt{\int_{f=0}^{\infty} S_{V_n} \left| T_n(j\omega) \right|^2 \, df}$$

Example: First-Order RC Network



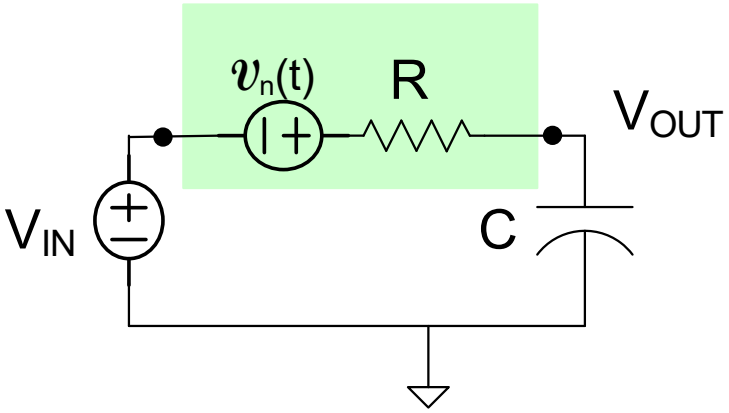
Noise transfer function:

$$T_n(s) = \frac{1}{1+RCs}$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{VOUT}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,df}$$

Example: First-Order RC Network

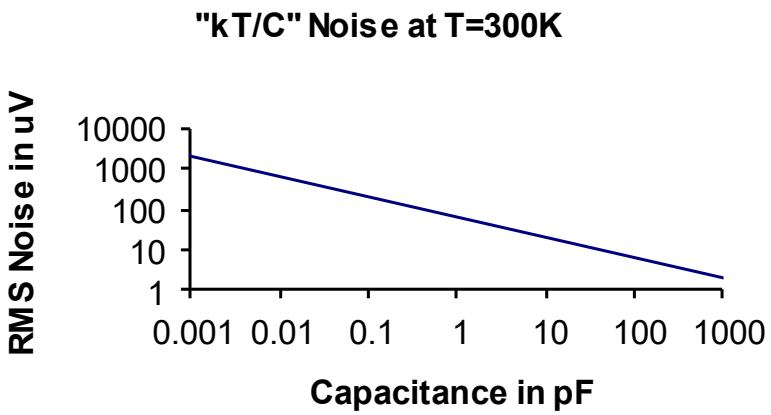


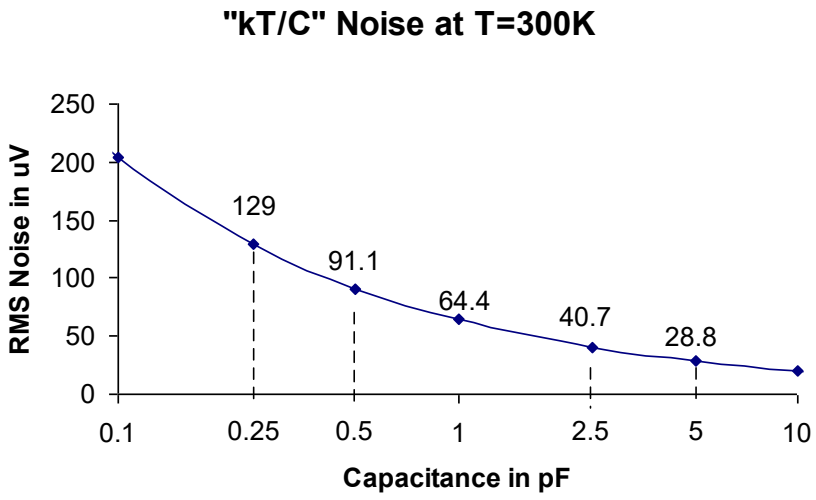
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\, df}$$

From a standard change of variable with a trig identity, it follows that

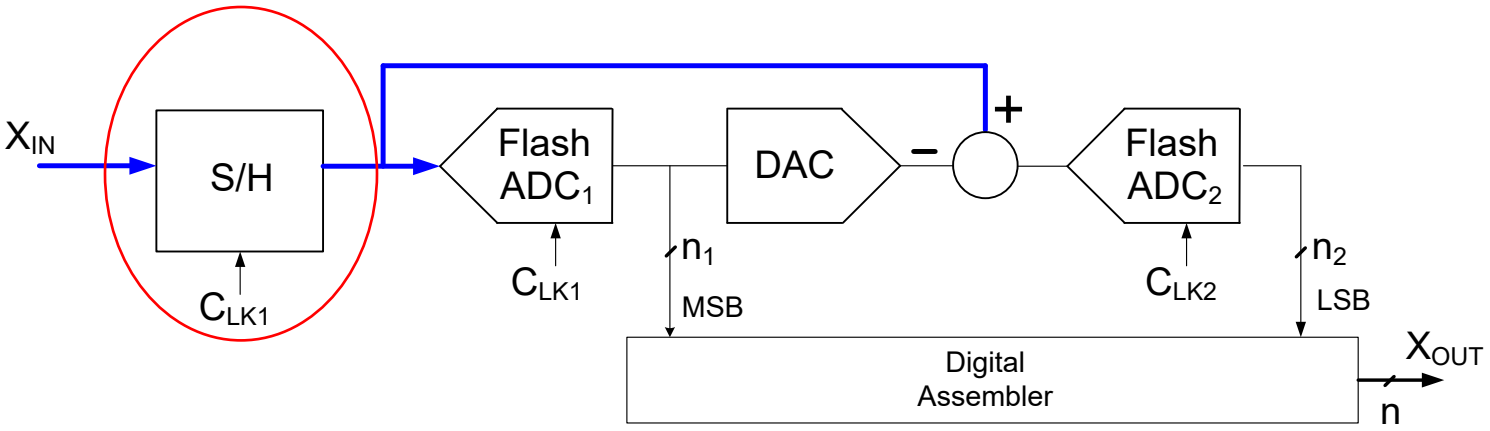
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$

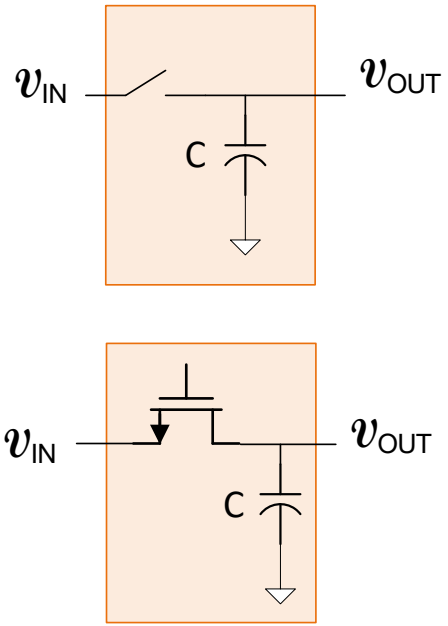
- The continuous-time noise voltage has an RMS value that is independent of R
- Noise contributed by the resistor is dependent only upon the capacitor value C
- This is often referred to at kT/C noise and it can be decreased at a given T only by increasing C


"kT/C" Noise at T=300K
RMS Noise in uV
10000
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Capacitance in pF


"kT/C" Noise at T=300K
RMS Noise in uV
250
200
150
100
50
0
129
91.1
64.4
40.7
28.8
0.1
0.25
0.5
1
2.5
5
10
Capacitance in pF

Sample and Hold Circuits





Basic S/H circuit

Slightly more complicated S/H used for input S/H

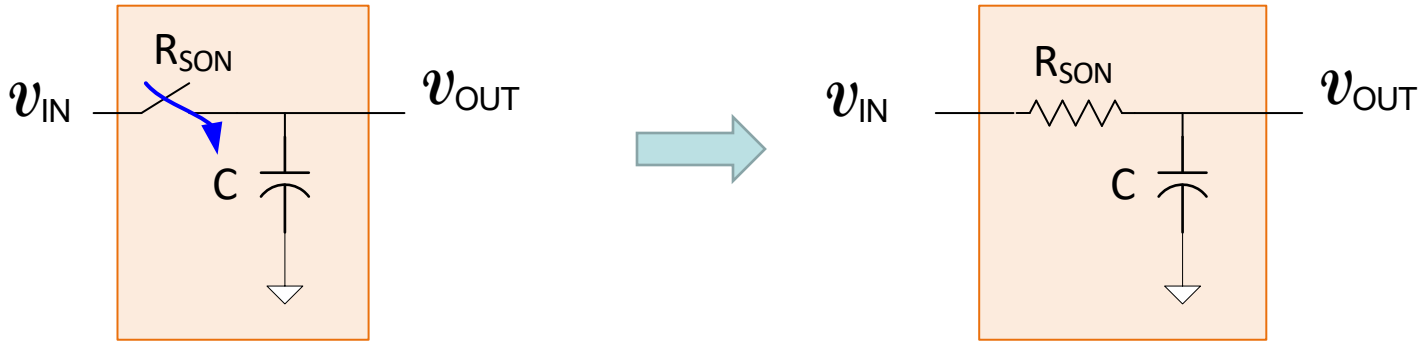
This simple structure used in some applications

Actually a Track and Hold Circuit

Noise characteristics of S/H similar to that of these simple samplers

Sample and Hold Circuits

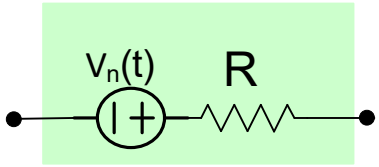
During Track Mode



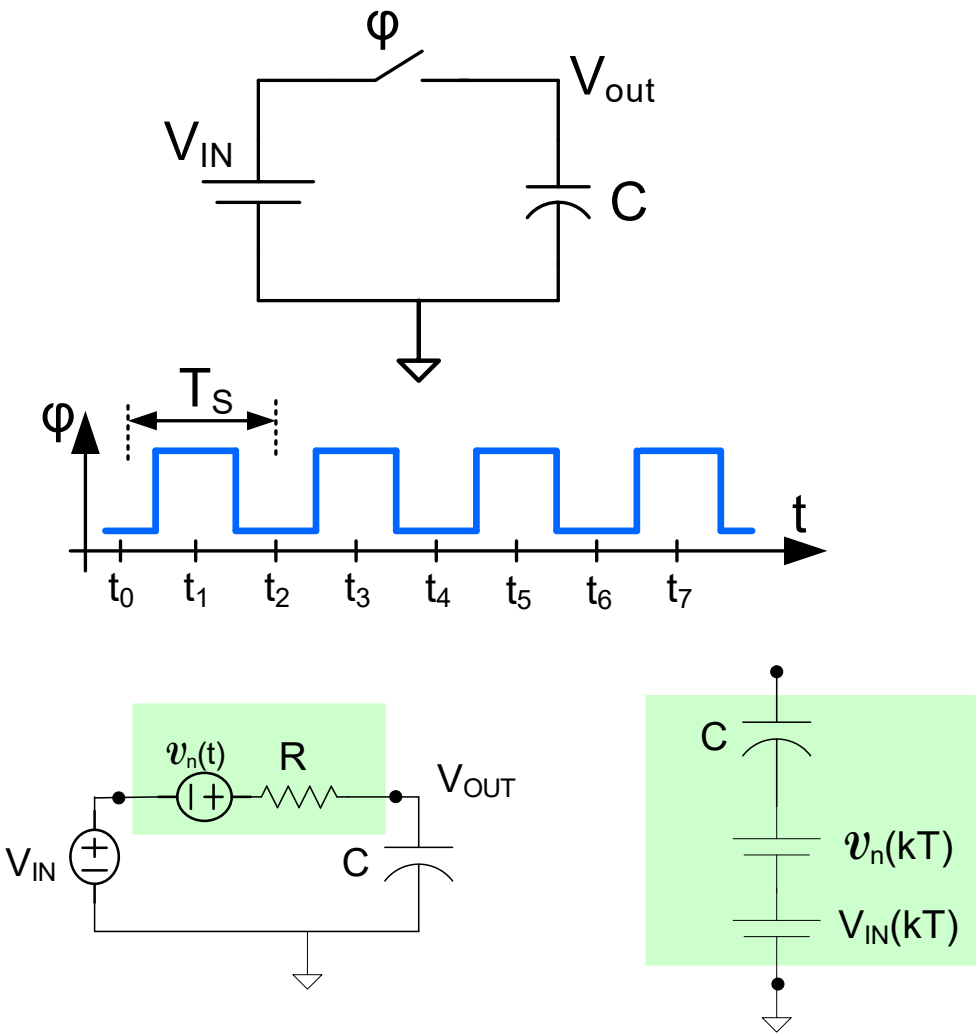
When switch is opened to take sample, noise on C is captured on C (superimposed on signal)

This noise becomes input noise to the ADC

Recall noise in resistor modeled as noise voltage source in series with R



Sample and Hold Circuits



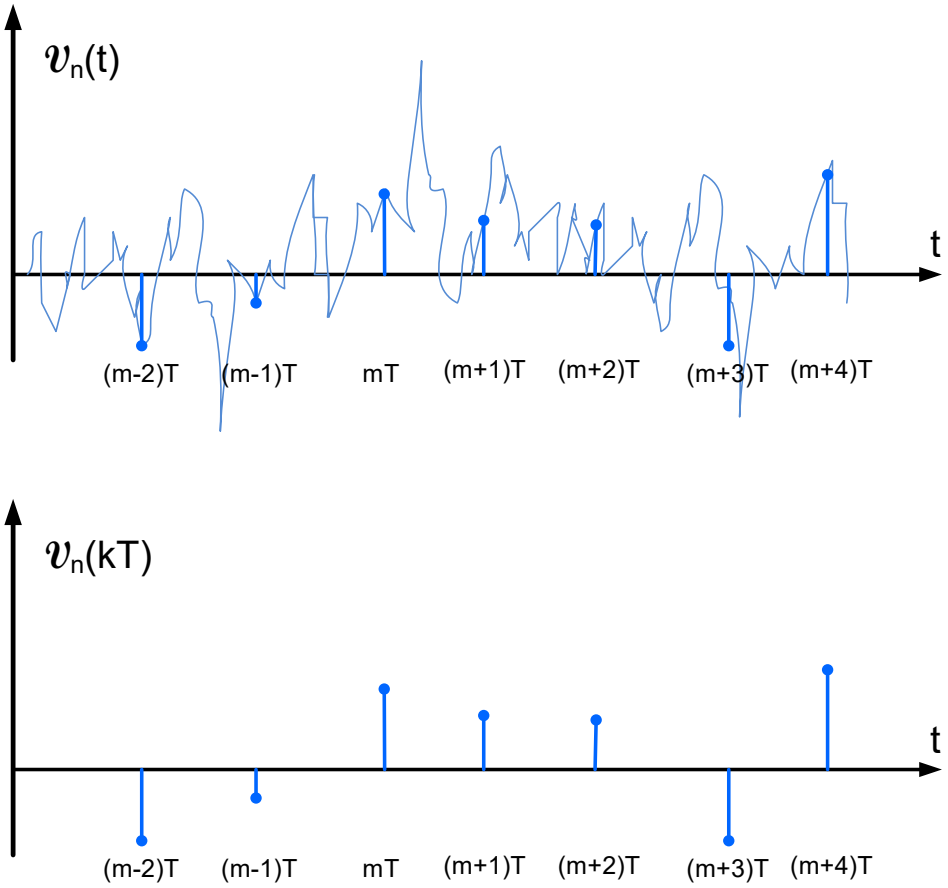
Track mode

Hold mode

If switch opens fast, noise on C due to R is captured as $v_n(kT)$

Sample and Hold Circuits

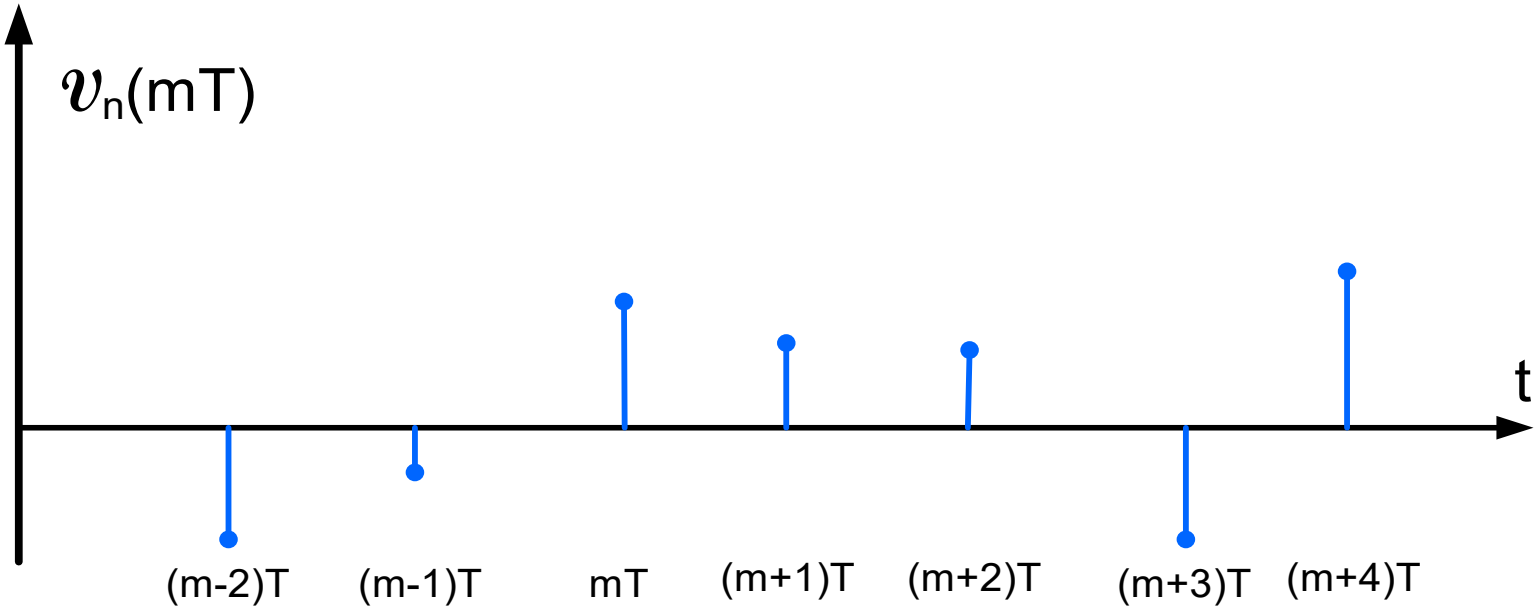
T is the period of the sampler



$v_n(mT)$ is a discrete-time sequence obtained by sampling continuous-time noise waveform

RMS value of noise input to pipelined ADC is that of the discrete time noise sequence

Sample and Hold Circuits



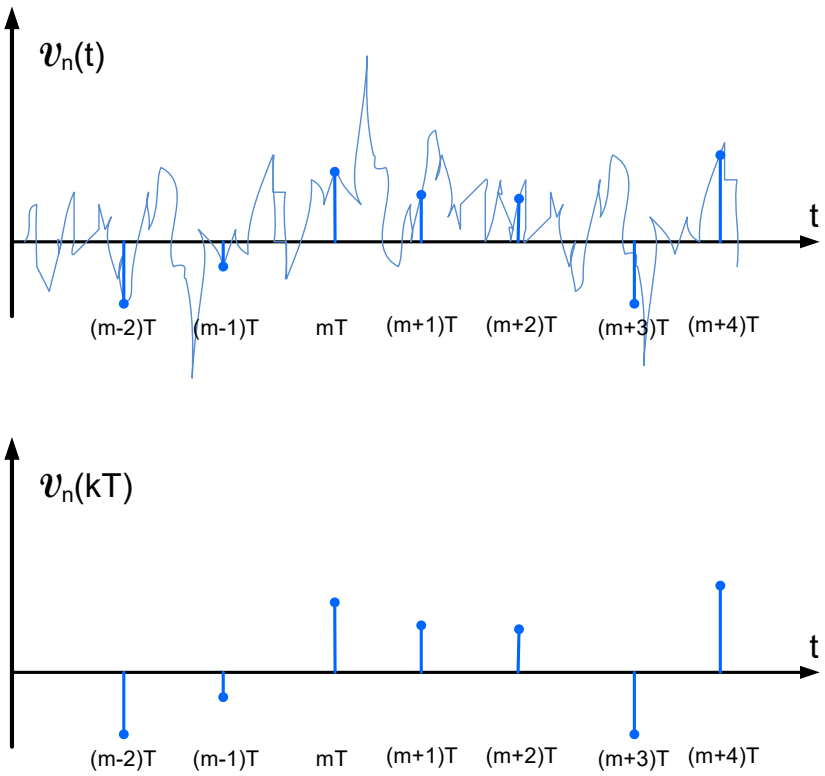
Define the RMS noise of a discrete time noise sequence as

$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right)$$

Thus:

$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right) \underset{N\,large}{\simeq} \sqrt{\frac{1}{N}\sum_{m=1}^{N} v^2(mT)}$$

Sample and Hold Circuits



$v_n(mT)$ for each m is a random variable with some distribution function

This distribution function is independent of m (i.e. the variables are identically distributed)

Assume μ_n is the mean and σ_n is the standard deviation of this random variable

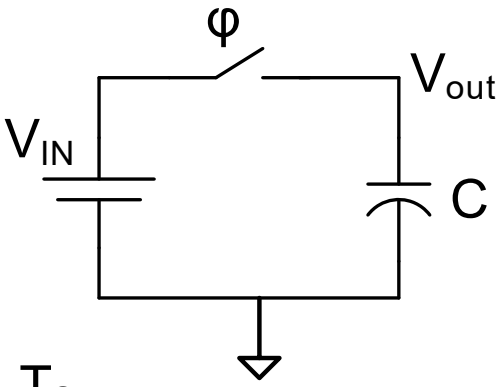
What is the relationship, if any, between $v_{n_{RMS}}$ and $\hat{v}_{RMS}$

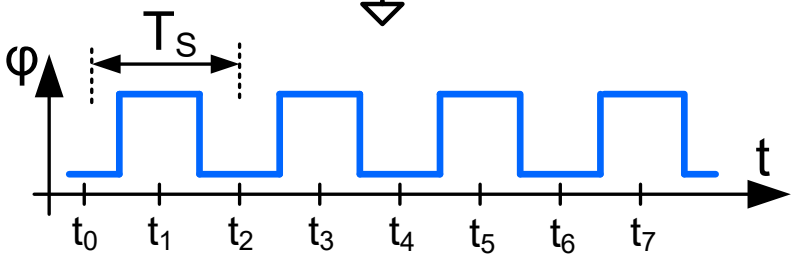
Theorem 1 If $v(t)$ is a continuous-time zero-mean noise source and $\langle v(kT) \rangle$ is a sampled version of $v(t)$ sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as $v_{RMS} = \hat{v}_{RMS}$

Theorem 2 If $v(t)$ is a continuous-time zero-mean noise signal and $\langle v(kT) \rangle$ is a sampled version of $v(t)$ sampled at times T, 2T, …. then the standard deviation of the random variable $v(kT)$, denoted as $\sigma_{\hat{V}}$ satisfies the expression $\sigma_{\hat{V}} = v_{RMS} = \hat{v}_{RMS}$

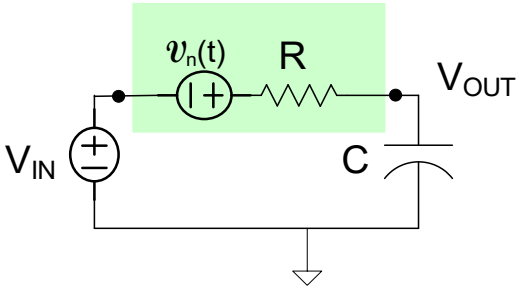
From Theorem 1 we obtain the RMS value of the switched capacitor sampler

Sample and Hold Circuits

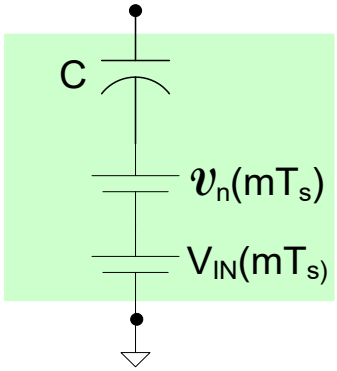




$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\frac{kT}{C}}$$



Track mode



Hold mode

$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

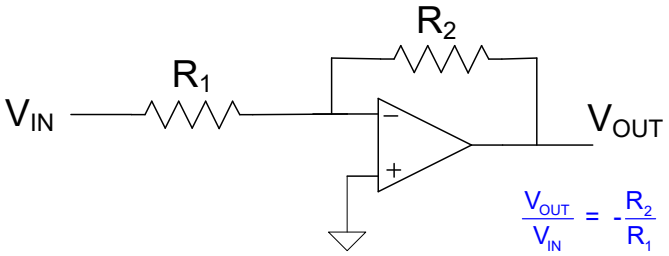
k: Boltzmann's constant
T: temperature in Kelvin

RMS noise at output of basic SC S/H is independent of R but dependent upon C

Amplifiers and Filter on Silicon

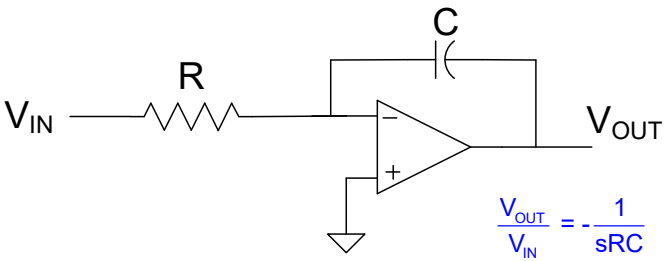
- Finite Gain Amplifiers
- Filters

Some of the most basic and widely used analog circuits



$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

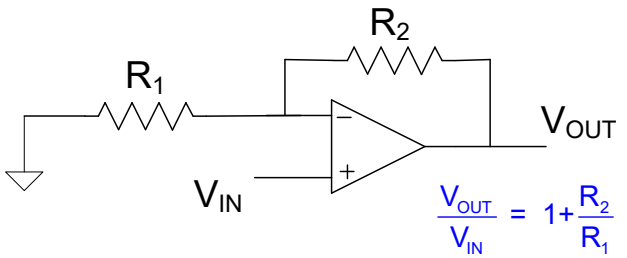
Inverting Amplifier



$$\frac{V_{OUT}}{V_{IN}} = -\frac{1}{sRC}$$

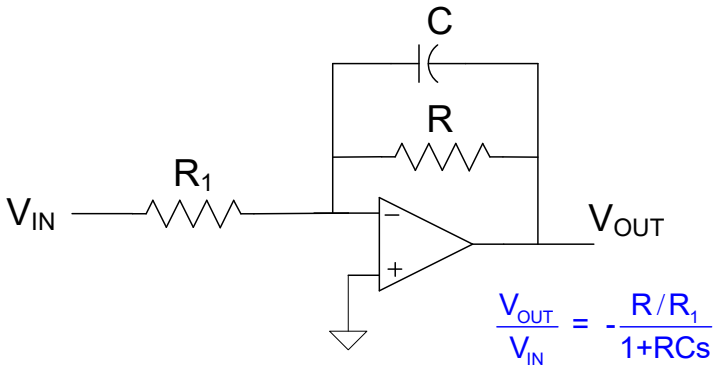
Inverting Integrator

$$I_0 = \frac{1}{RC}$$



$$\frac{V_{OUT}}{V_{IN}} = 1+\frac{R_2}{R_1}$$

Noninverting Amplifier



$$\frac{V_{OUT}}{V_{IN}} = -\frac{R/R_1}{1+RCs}$$

Low-pass Active Filter

$$p = -\frac{1}{RC}$$

Not practical to implement on silicon

- Area for R too big
- Area for C too big
- Accuracy of I_0 and p too poor

But ratio accuracy can be very good (0.1% or better with good layout and appropriate area)

How bad is the problem?

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

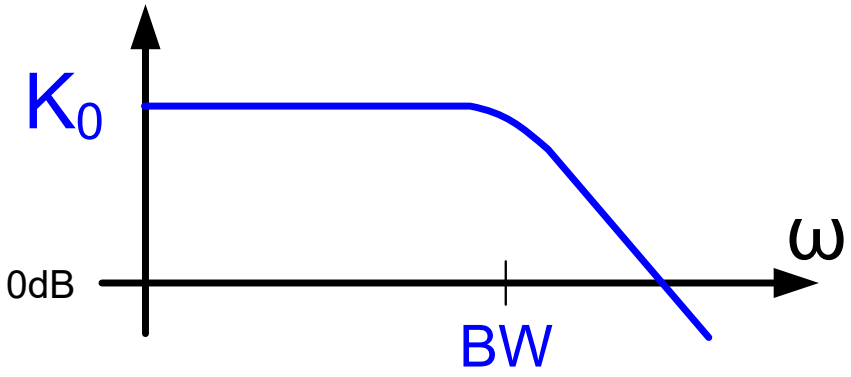
PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

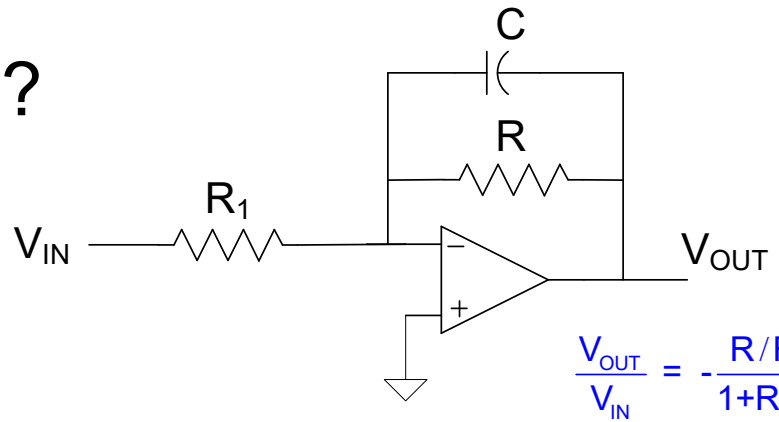
COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

$R_{\square}=21.7\Omega/\square$ and $Cd=0.864fF/\mu^2$

How bad is the problem?





Low-pass Active Filter

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R/R_1}{1+RCs}$$

$$p = -\frac{1}{RC}$$

$$K_0 = 1+\frac{R_2}{R_1}$$

$$BW_{rad/sec} = -p = \frac{1}{RC}$$

Assume |p|=2π•1000 and pole accuracy needed is 0.1%

Process tolerance on R and C is about ±20%

R□=20Ω/□ and Cd=1pF/μ² (approximately)

If R=1KΩ, require 1000/20=50 squares

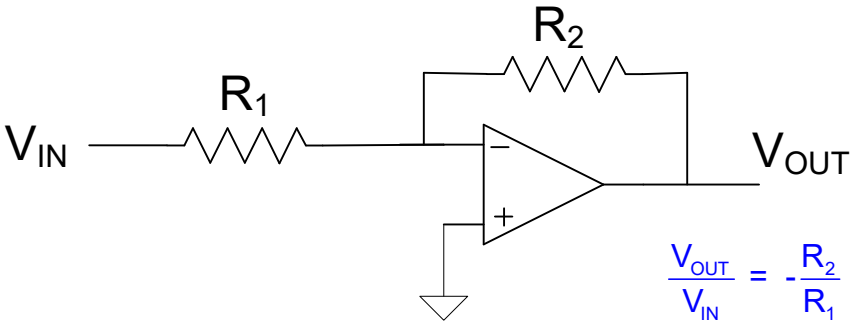
$$\frac{1}{RC} = 2000\pi \qquad C = \frac{1}{R\bullet 2000\pi} \qquad C = \frac{1}{1000 \bullet 2000\pi} = 0.159\mu F$$

$$A_C = \frac{C}{C_D} = \frac{0.159\mu F}{1fF/\mu^2} = 1.59\times 10^8 \mu^2$$

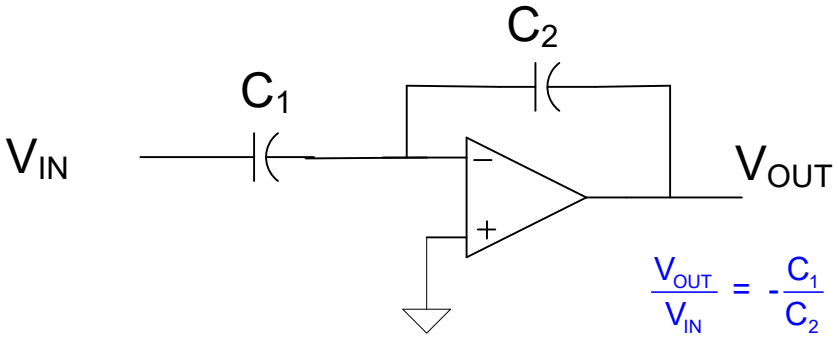
Pole tolerance ±40%

Both are orders of magnitude unacceptable !

An amplifier alternative ?



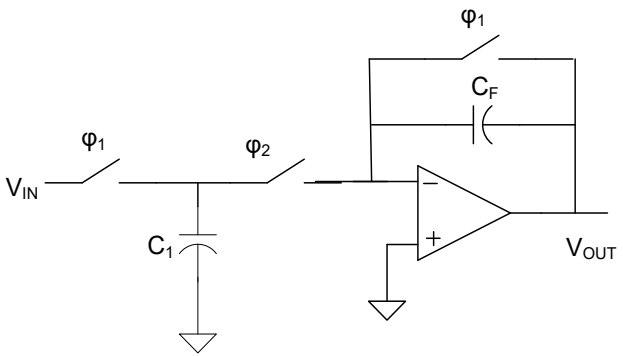
Inverting Amplifier

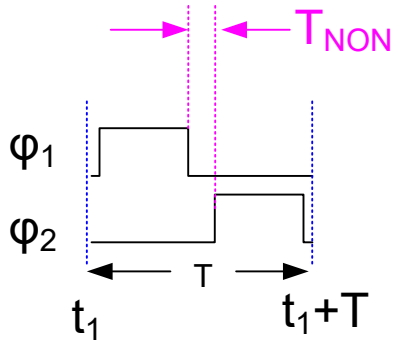


Inverting Amplifier

- Capacitor version is area effective and can have very good accuracy
- The node between C_1 and C_2 is a floating node if the Op Amp has a MOS differential pair at the input
- But if we get any charge on the intermediate node there is no way to get it off

An amplifier alternative ?:





Φ_1 and Φ_2 are nonoverlapping clocks

During Φ_1

C_1 is charged to V_{IN} and stores charge $Q_1=C_1V_{IN}$

C_F is discharged and $V_{OUT}=0$

During Φ_2

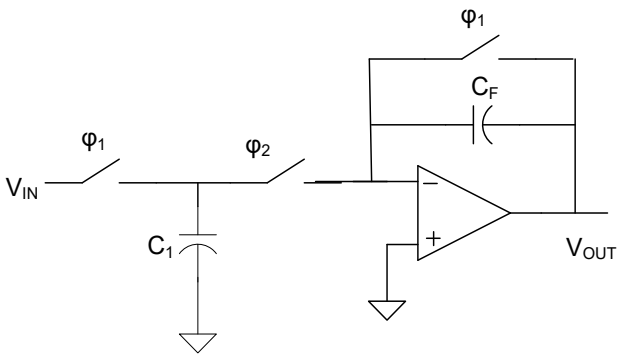
C_1 is discharged but charge is transferred to C_F

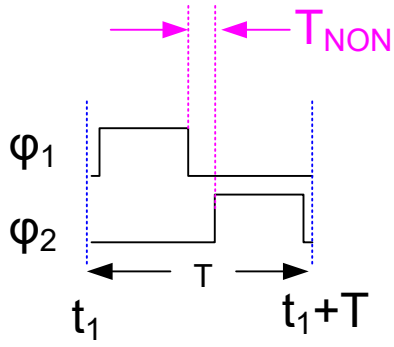
$Q_2=-Q_1$ and $V_{OUT}=Q_2/C_F$

Substituting for Q_1 we obtain $V_{OUT} = -\frac{C_1}{C_F} V_{IN}$

Serves as a voltage amplifier with output valid during φ_2

An amplifier alternative !





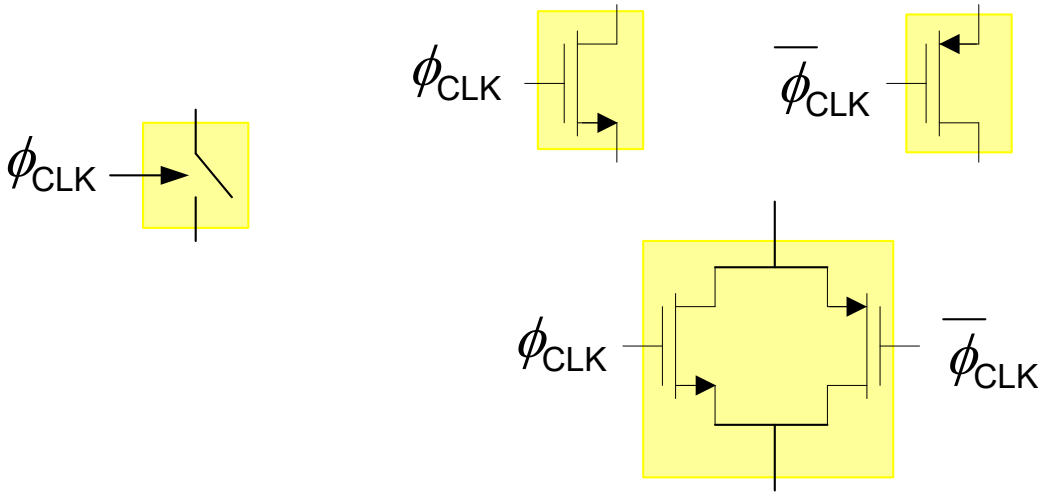
Φ_1 and Φ_2 are nonoverlapping clocks

$$V_{OUT} = -\frac{C_1}{C_F} V_{IN}$$

- Many applications only need amplifier output at discrete points in time
- Accuracy can be very good
- Area can be very small

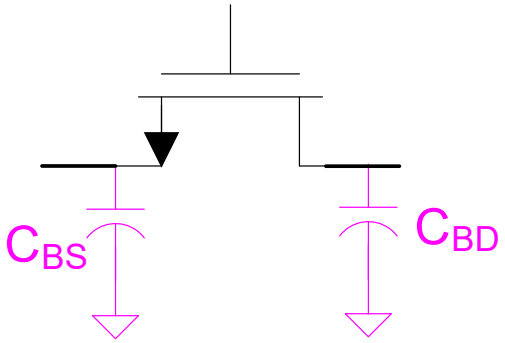
But, what about the switches?

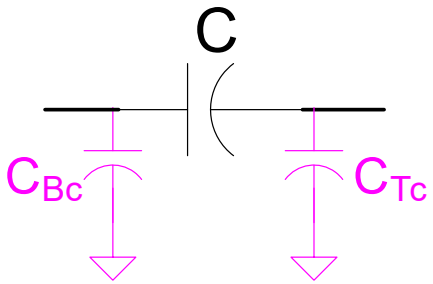
Switches for SC Circuits



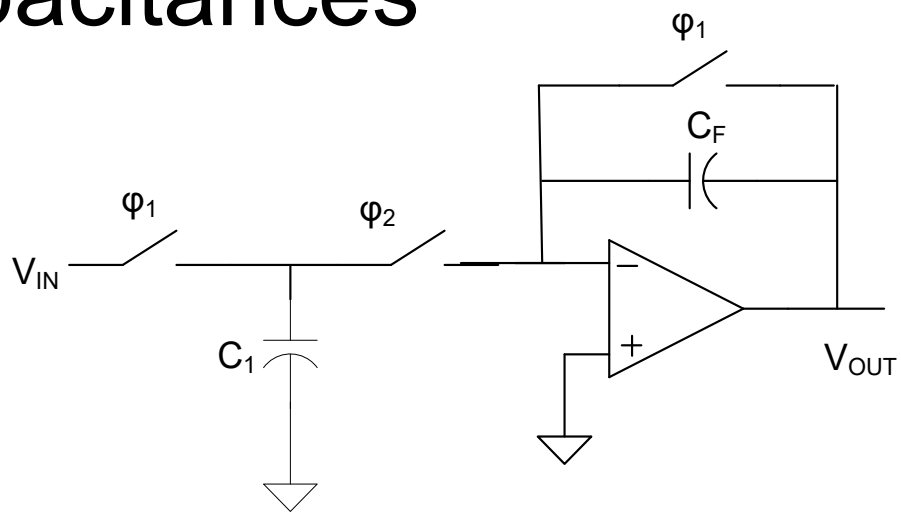
- Often a single MOS transistor is adequate (either n-ch or p-ch)
- Sometimes need transmission-gate switch (parallel n-ch and p-ch)
- Switches work very well and can be very small but must manage their R_{ON}

Parasitic Capacitances





?



3 switches and 2 capacitors

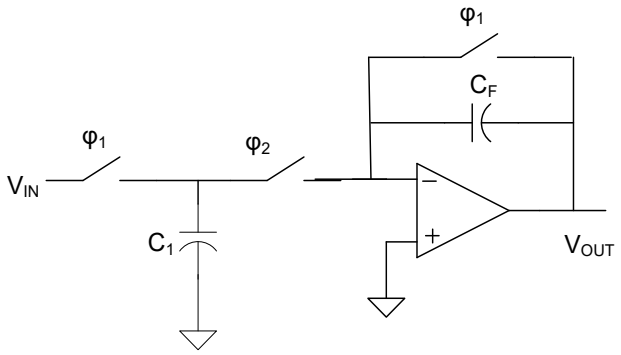
10 parasitic capacitances!

Some of parasitic capacitances may be several percent of the size of C_1 and C_F

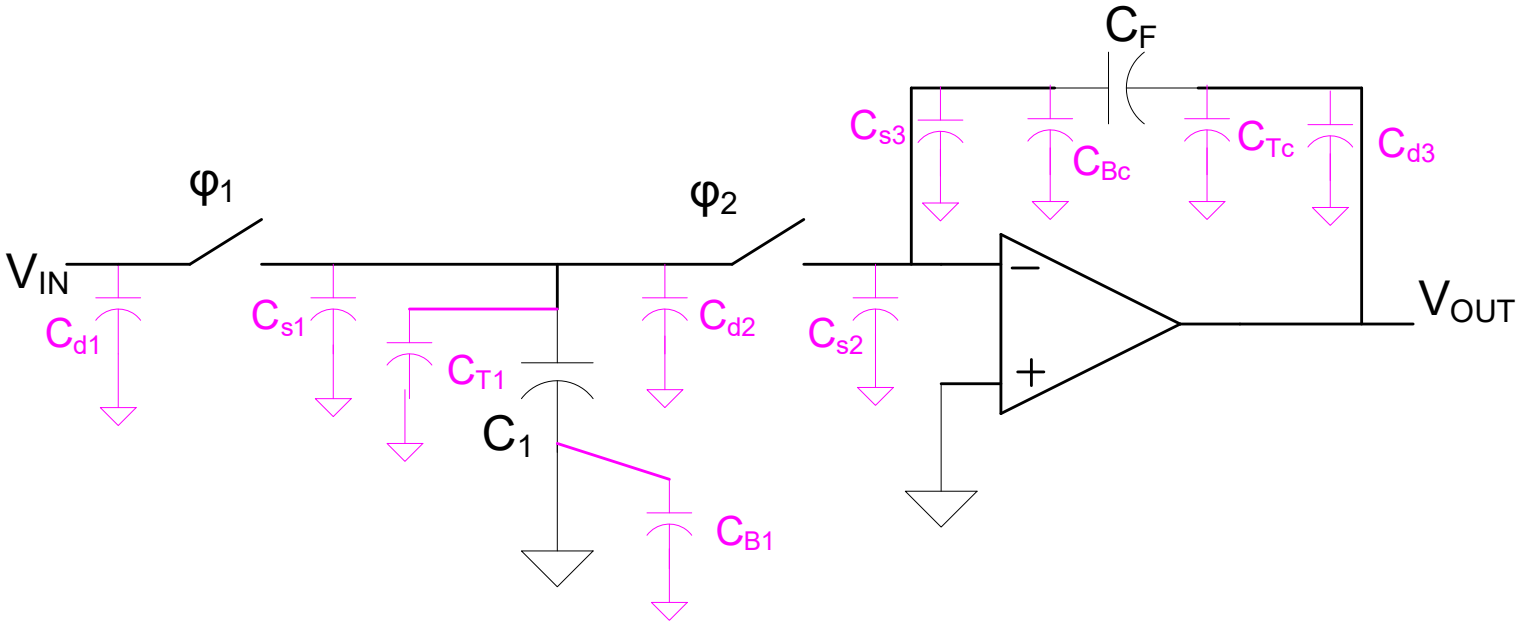
And parasitic capacitors do not match very well

And parasitic capacitances may be highly nonlinear (junction capacitors)

Parasitic Capacitances

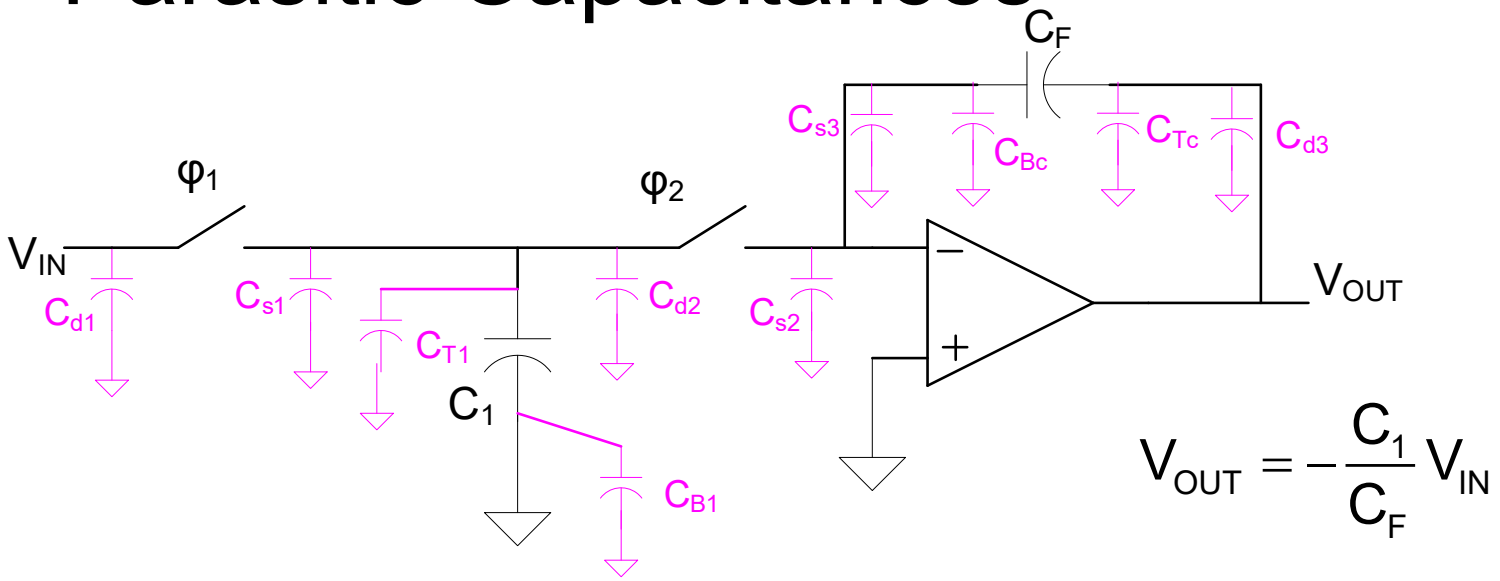


Ideally $V_{OUT} = -\frac{C_1}{C_F} V_{IN}$



10 parasitic capacitances!

Parasitic Capacitances



C_1/C_F can be very precisely controlled with appropriate layout and area allocation

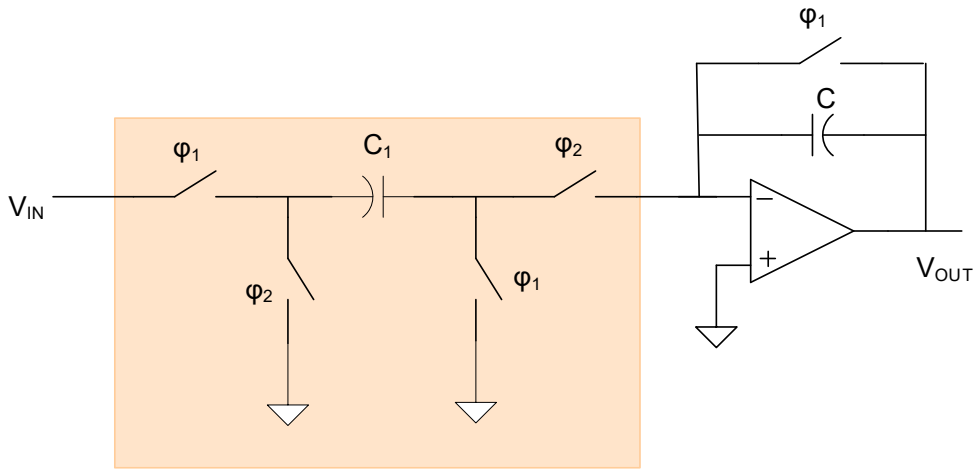
If op amp is ideal, C_{d1}, C_{B1},C_{s2},C_{s3},C_{Bc},C_{Tc} and C_{d3} do not affect charge transfer !

But C_{s1},C_{T1},C_{d2} are all in parallel with C_1 and all transfer charge

$$V_{OUT} = -\frac{C_1 + (C_{s1} + C_{T1} + C_{d2})}{C_F} V_{IN}$$

Parasitic capacitances not accurately controlled and dramatically degrade matching!

Stray Insensitive SC Amplifiers

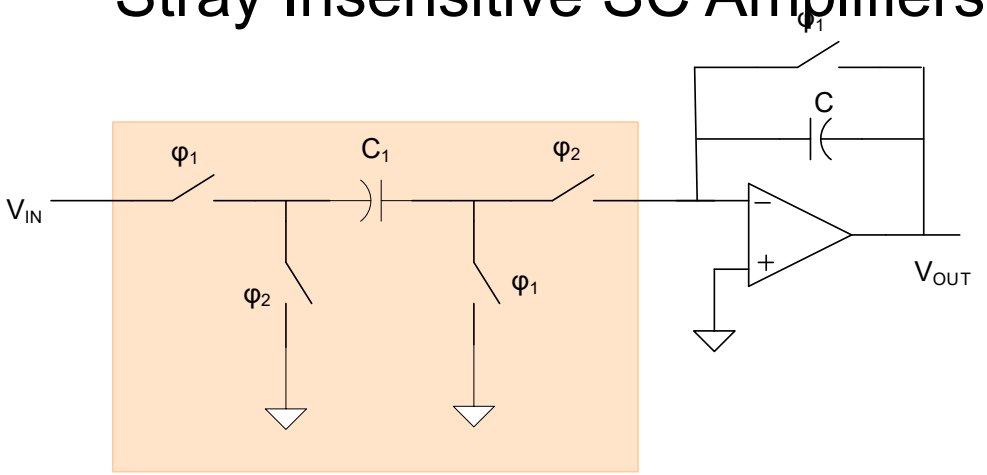


Noninverting

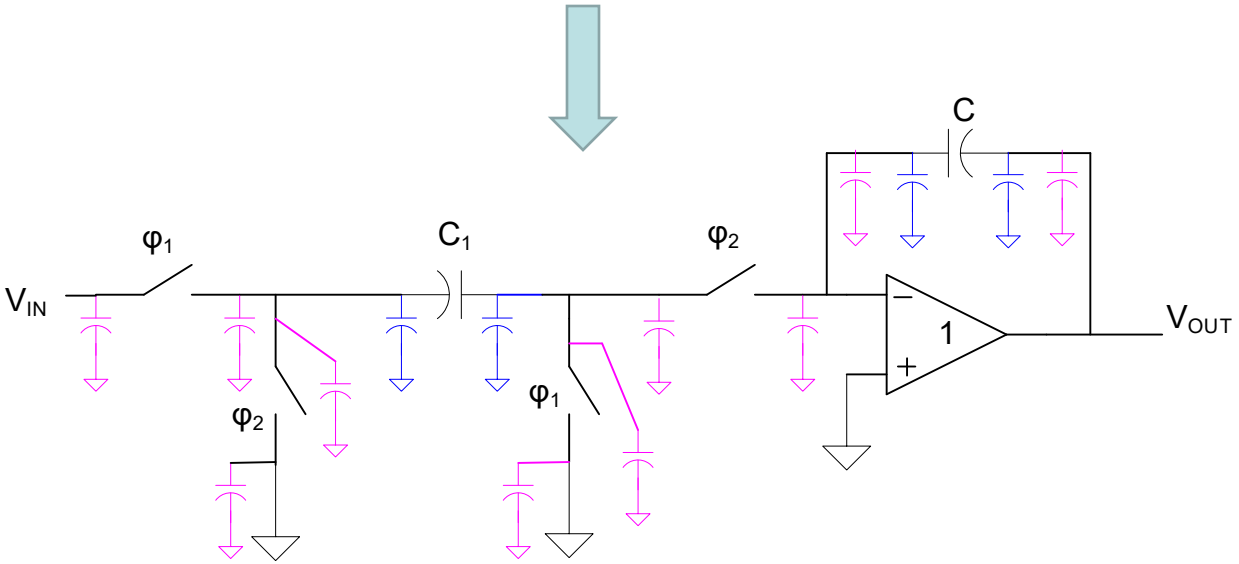
Another SC Amplifier with even more switches !

Increased to 14 diffusion parasitic capacitances

Stray Insensitive SC Amplifiers

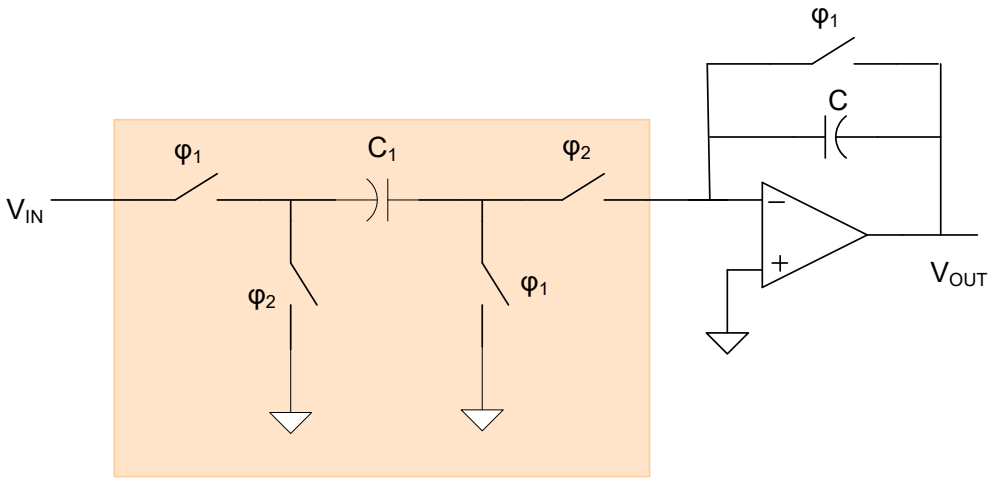


Noninverting



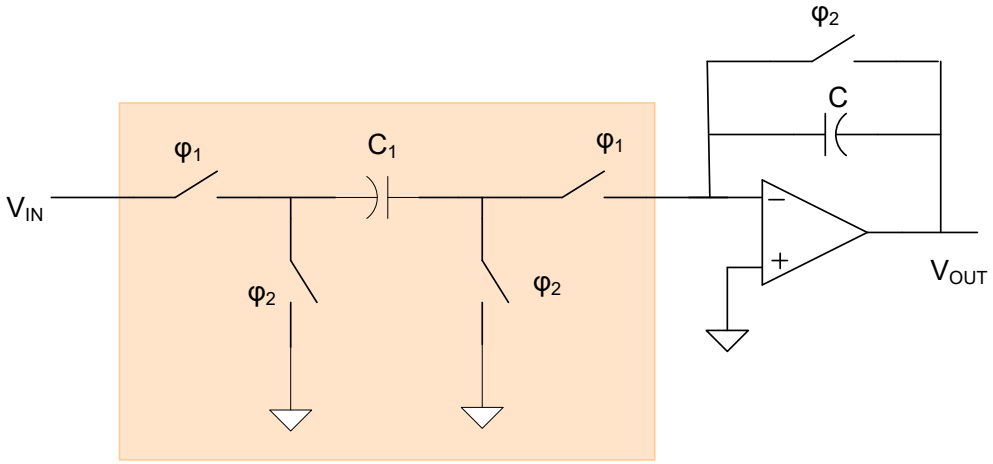
Can show that all 14 diffusion parasitic capacitances do not affect gain !!

Stray Insensitive SC Amplifiers



Noninverting

$$\frac{V_{OUT}}{V_{IN}} = \frac{C_1}{C_2}$$

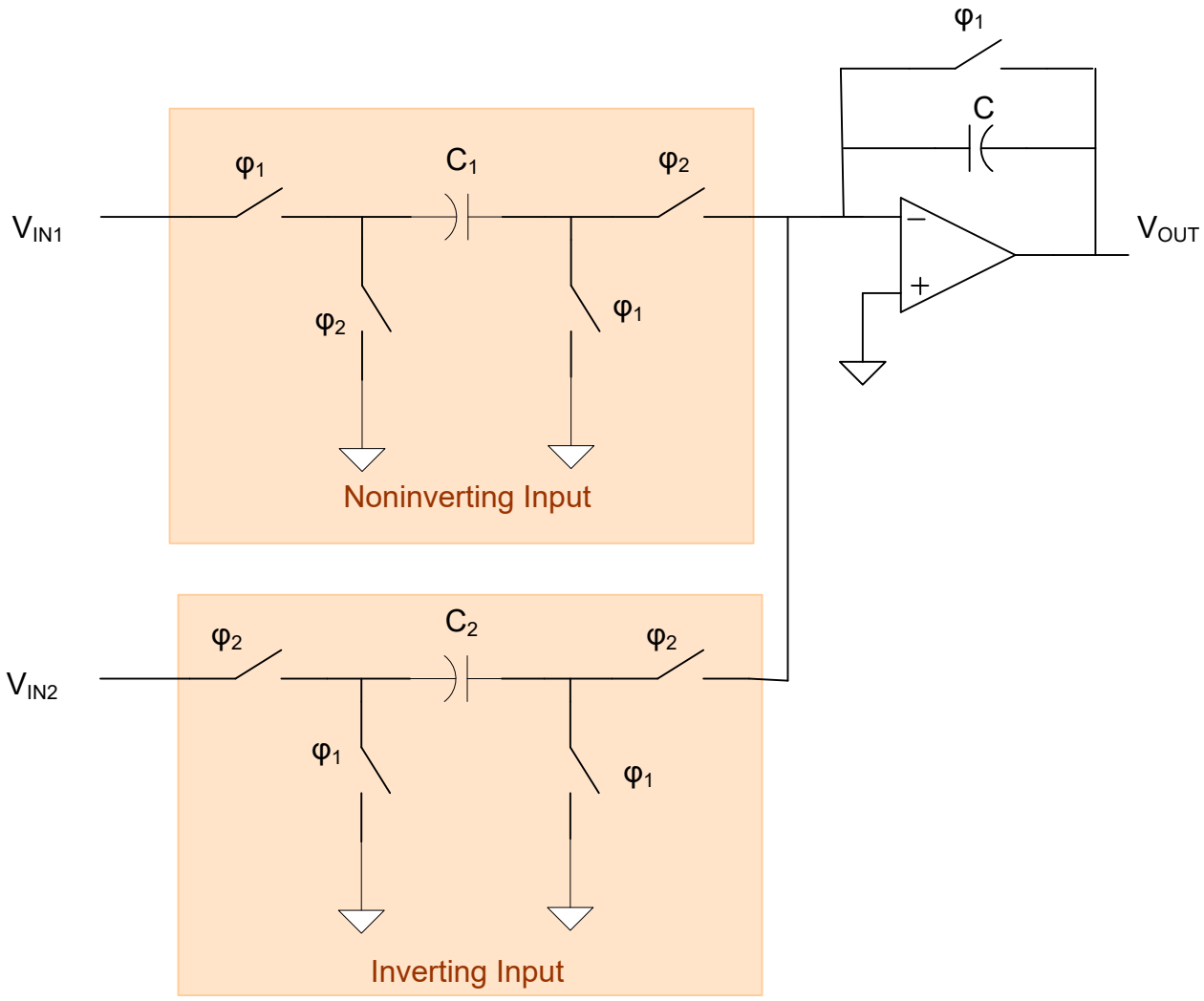


Ininverting

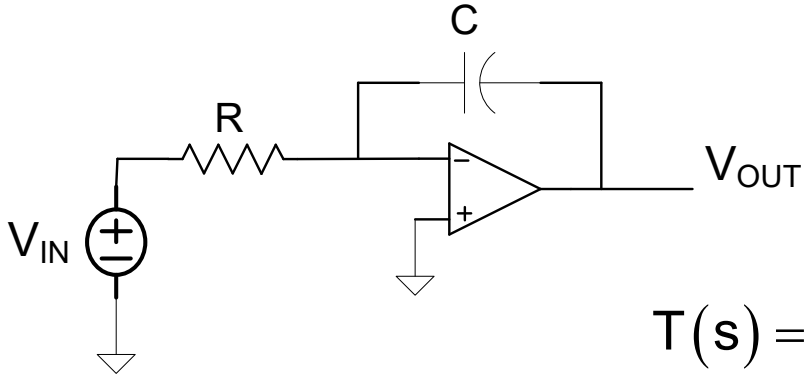
$$\frac{V_{OUT}}{V_{IN}} = -\frac{C_1}{C_2}$$

Can show that all diffusion parasitic capacitances do not affect gain
Gain can be accurately controlled !

Summing amplifier inputs either inverting or noninverting can be easily obtained



Consider the Basic Integrator



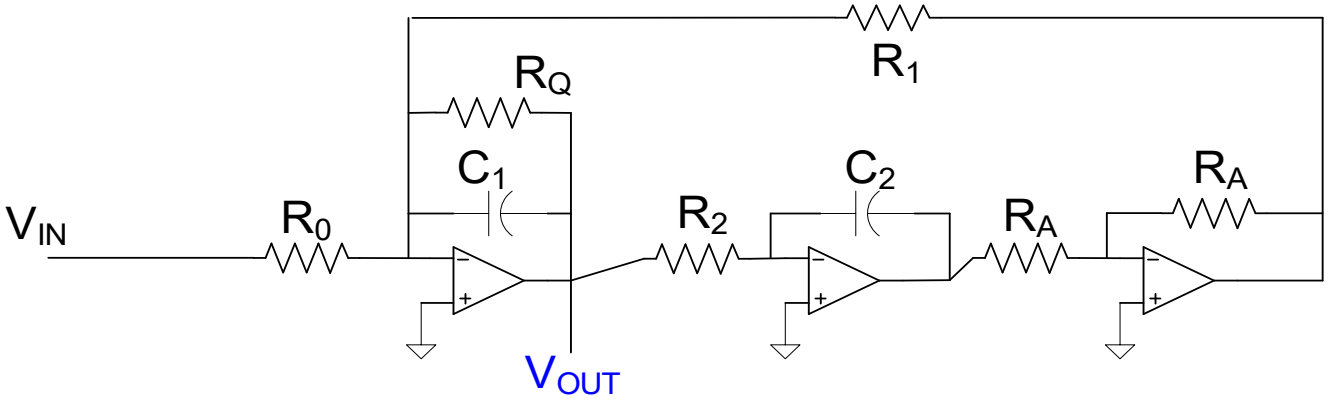
$$T(s) = -\frac{1}{RCs}$$

$$I_0 = \frac{1}{RC}$$

Key performance of integrator (and integrator-based filters) is determined by the integrator time constant I_0

Precision of time constants of a filter invariably determined by precision of I_0

Integrator-Based Filters:

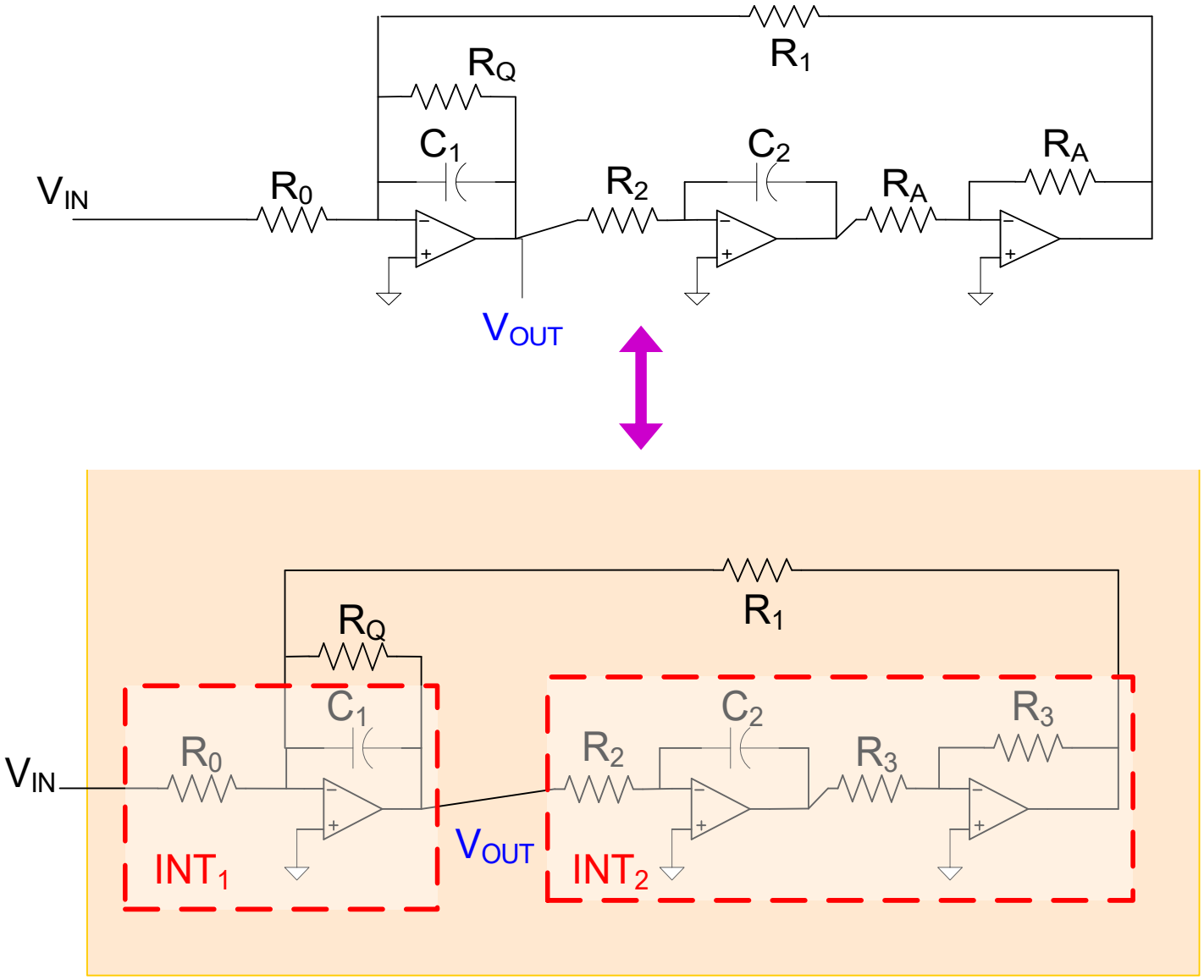


$$\frac{V_{OUT}}{V_{IN}} = T(s) = -\frac{1}{R_0 C_1} \frac{s}{s^2 + s\left(\frac{1}{R_Q C_2}\right) + \frac{1}{R_1 R_2 C_1 C_2}}$$

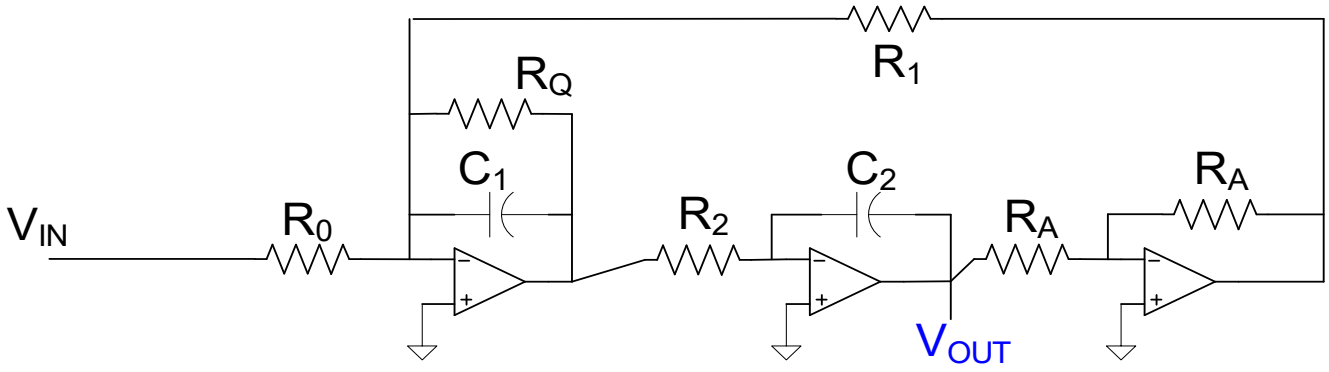
Second-order Bandpass Filter

Denote as a two-integrator-loop structure

Integrator-Based Filters:



Integrator-Based Filters:



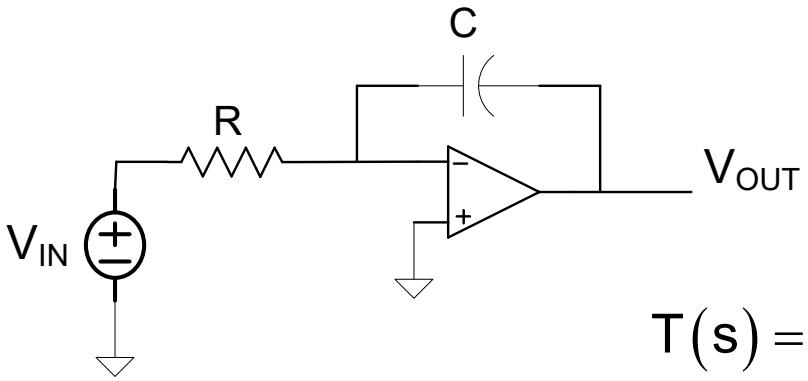
$$\frac{V_{OUT}}{V_{IN}} = T(s) = -\frac{1}{R_0 C_1} \frac{\frac{1}{R_2 C_2}}{s^2 + s\left(\frac{1}{R_Q C_2}\right) + \frac{1}{R_1 R_2 C_1 C_2}}$$

Second-order Lowpass Filter

Denote as a two-integrator-loop structure

- Any filter transfer function can be implemented with integrators and summers
- Some of the best known filter structures are based upon integrators and summers
- Accuracy of RC products is critical in the design of good filters

Consider the Basic Integrator



$$T(s) = -\frac{1}{RCs}$$

$$I_0 = \frac{1}{RC}$$

Accurate control of I_0 is required to build good filters !

1. Accuracy of R and C difficult to accurately control – particularly in integrated applications (often 2 or 3 orders of magnitude to variable)

2. Size of R and C unacceptably large if I_0 is in audio frequency range (2 or 3 orders of magnitude too large)

3. Amplifier GB limits performance

Appears to be Incredible Challenge to Building Filters on Silicon!

Stay Safe and Stay Healthy !

End of Lecture 40